OBLON
SPIVAK
MCCLELLAND
MAIER
&
NEUSTADT
P.C.

ATTORNEYS AT LAW

Docket No.: 252069US2

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

RE: Application Serial No.: 10/826,391
Applicants: Hideki TAKAHASHI, et al.
Filing Date: April 19, 2004
For: INSULATED GATE BIPOLAR TRANSISTOR WITH BUILT-IN FREEWHEELING DIODE
Group Art Unit: 2815
Examiner: LANDAU, M.C.

SIR:

Attached hereto for filing are the following papers:

APPEAL BRIEF

Our credit card payment form in the amount of **$500.00** is attached covering any required fees. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Registration No. 28,870

Zachary S. Stern
Registration No. 54,719

Customer Number
22850
(703) 413-3000 (phone)
(703) 413-2220 (fax)

DOCKET NO: 252069US2

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
HIDEKI TAKAHASHI, ET AL.	: EXAMINER: LANDAU, M. C.
SERIAL NO: 10/826,391	:
FILED: APRIL 19, 2004	: GROUP ART UNIT: 2815
FOR: INSULATED GATE BIPOLAR TRANSISTOR WITH BUILT-IN FREEWHEELING DIODE	:

APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

This is an appeal of the Advisory Action mailed July 31, 2006 and the Final Action mailed April 18, 2006 that presented a final rejection of Claims 2-6 and 13-15. A Notice of Appeal was timely filed with a one month extension on August 14, 2006.

I. REAL PARTY IN INTEREST UNDER 37 C.F.R. § 41.37(c)(1)(i)

The real party in interest in this appeal is the Assignee, MITSUBISHI DENKI KABUSHIKI KAISHA, having a place of business at 2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo, Japan 100-8310.

II. RELATED APPEALS AND INTERFERENCES UNDER 37 C.F.R. § 41.37(c)(1)(ii)

Appellant, Appellant's legal representative, and the Assignee are aware of no appeals that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS UNDER 37 C.F.R. § 41.37(c)(1)(iii)

Claims 2-17 are pending in this application. Claims 7-12, 16 and 17 were withdrawn from consideration due to a previous restriction requirement, and Claims 2-6 and 13-15 were finally rejected and form the basis for this appeal. Claim 1 was previously canceled. The attached claim appendix includes a clean copy of pending Claims 2-17.

IV. STATUS OF THE AMENDMENTS UNDER 37 C.F.R. § 41.37(c)(1)(iv)

No amendments were filed after the final rejection, mailed April 18, 2006.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER UNDER 37 C.F.R. § 41.37(c)(1)(v)

Independent Claim 2 is directed to an insulated gate bipolar transistor (IGBT). Appellant's FIG. 2 shows a longitudinal sectional view of a non-limiting embodiment of an IGBT according to Claim 2. However, the claims should not be considered to be limited to the embodiment shown in this example.

The IGBT of Claim 2 includes a semiconductor substrate of a first conductivity type (e.g., n- semiconductor substrate layer 1 having an n conductivity type, in FIG. 2). The semiconductor substrate in this example includes a first main surface 1S1 and a second main surface 1S2.

Further, the IGBT of Claim 2 includes an insulated gate transistor (e.g., an N-type channel MOSFET, see Specification at page 11, lines 17-20) formed in a region of

semiconductor substrate 1 on a side where the first main surface 1S1 is included. The insulated gate transistor includes a channel of the first conductivity type (e.g., N-type channel) which is formed within a base region of a second conductivity type (e.g., p-type base region 2) during an on state of the insulated gate transistor. The base region 2 extends from first main surface 1S1 toward an interior of the semiconductor substrate 1 (see FIG. 2 and Specification at page 11, line 22, to page 12, line 1).

Further, the IGBT of Claim 2 includes a first main electrode (e.g., electrode 7) formed on the first main surface 1S1 and being in contact with the base region 2 of the insulated gate transistor at the first main surface 1S1 (see FIG. 2 and Specification at page 12, lines 18-22).

Further, the IGBT of Claim 2 includes a first semiconductor layer (e.g., layer 8) of the first conductivity type (e.g, n^+ type) formed on the second main surface 1S2 of the semiconductor substrate 1 and facing the insulated gate transistor (see FIG. 2 and Specification at page 12, lines 23-25).

In addition, the IGBT of Claim 2 includes a second semiconductor layer (e.g., layer 9) of the second conductivity type (e.g., p^+ type) formed on the second main surface 1S2 of the semiconductor substrate 1 and facing the insulated gate transistor (see FIG. 2 and Specification at page 13, lines 1-6).

Moreover, the IGBT of Claim 2 includes a second main electrode (e.g., electrode 10) formed on the first semiconductor layer 8 and the second semiconductor layer 9 (see FIG. 2 and Specification at page 13, lines 7-9). An interface IF between the second main electrode 10 and each of the first semiconductor layer 8 and the second semiconductor layer 9 is parallel to the first main surface 1S1 (see FIG. 2 and Specification at page 13, lines 9-11).

Further, a distance D between the first main surface 1S1 and the interface IF is equal to 200 μm or smaller (see FIG. 2 and Specification at page 13, lines 16-17).

In addition, a thickness T8/T9 of each of the first semiconductor layer 8 and the second semiconductor layer 9 is equal to 2 μm or smaller (see FIG. 2 and Specification at page 13, lines 17-19).

Further, a first interface IF1 between the first semiconductor layer 8 and the second main electrode 10 occupies 20-70% of the interface IF between the second main electrode 10 and each of the first semiconductor layer 8 and the second semiconductor layer 9 (see FIG. 2 and Specification at page 13, lines 19-23).

Independent Claim 3 is directed to an insulated gate bipolar transistor (IGBT). Appellant's FIG. 2 shows a longitudinal sectional view of a non-limiting embodiment of an IGBT according to Claim 3. However, the claims should not be considered to be limited to the embodiment shown in this example.

The IGBT of Claim 3 includes a semiconductor substrate of a first conductivity type (e.g., n- semiconductor substrate layer 1 having an n conductivity type, in FIG. 2). The semiconductor substrate in this example includes a first main surface 1S1 and a second main surface 1S2.

Further, the IGBT of Claim 3 includes an insulated gate transistor (e.g., an N-type channel MOSFET, see Specification at page 11, lines 17-20) formed in a region of semiconductor substrate 1 on a side where the first main surface 1S1 is included. The insulated gate transistor includes a channel of the first conductivity type (e.g., N-type channel) which is formed within a base region of a second conductivity type (e.g., p-type base region 2) during an on state of the insulated gate transistor. The base region 2 extends from first main surface 1S1 toward an interior of the semiconductor substrate 1 (see FIG. 2 and Specification at page 11, line 22, to page 12, line 1).

Further, the IGBT of Claim 3 includes a first main electrode (e.g., electrode 7) formed on the first main surface 1S1 and being in contact with the base region 2 of the insulated gate transistor at the first main surface 1S1 (see FIG. 2 and Specification at page 12, lines 18-22).

Further, the IGBT of Claim 3 includes a first semiconductor layer (e.g., layer 8) of the first conductivity type (e.g., n^+ type) formed on the second main surface 1S2 of the semiconductor substrate 1 and facing the insulated gate transistor (see FIG. 2 and Specification at page 12, lines 23-25).

In addition, the IGBT of Claim 3 includes a second semiconductor layer (e.g., layer 9) of the second conductivity type (e.g., p^+ type) formed on the second main surface 1S2 of the semiconductor substrate 1 and facing the insulated gate transistor (see FIG. 2 and Specification at page 13, lines 1-6).

Moreover, the IGBT of Claim 3 includes a second main electrode (e.g., electrode 10) formed on the first semiconductor layer 8 and the second semiconductor layer 9 (see FIG. 2 and Specification at page 13, lines 7-9). An interface IF between the second main electrode 10 and each of the first semiconductor layer 8 and the second semiconductor layer 9 is parallel to the first main surface 1S1 (see FIG. 2 and Specification at page 13, lines 9-11).

Further, a distance D between the first main surface 1S1 and the interface IF is equal to 200 μm or smaller (see FIG. 2 and Specification at page 13, lines 16-17).

In addition, a thickness T8/T9 of each of the first semiconductor layer 8 and the second semiconductor layer 9 is equal to 2 μm or smaller (see FIG. 2 and Specification at page 13, lines 17-19).

Further, a second interface IF2 between the second semiconductor layer 9 and the second main electrode 10 occupies 30-80% of the interface IF between the second main electrode 10 and each of the first semiconductor layer 8 and the second semiconductor layer 9 (see FIG. 2 and Specification at page 13, lines 19-23).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL UNDER 37 C.F.R. § 41.37(c)(1)(vi)

A) Claims 2-4, 6, 13 and 15 were finally rejected under 35 U.S.C. § 103(a) as unpatentable over Akiyama et al., "Effects of Shorted Collector on Characteristics of IGBTs" (herein "Akiyama") in view of U.S. Publication No. 2001/0040255 to Tanaka; and Claims 5 and 14 were finally rejected under 35 U.S.C. § 103(a) as unpatentable over Akiyama in view of Tanaka and U.S. Patent No. 6,798,040 to Reznik.

B) Claims 1-3, 6 and 15 were finally rejected under 35 U.S.C. § 103(a) as unpatentable over Tanaka.

VII. ARGUMENTS UNDER 37 C.F.R. § 41.37(c)(1)(vii)

A) Akiyama and Tanaka fail to teach or suggest a distance between a first main surface and an interface is 200 μm or less, as recited in Claims 2 and 3.

Appellant respectfully submits that the rejection of Claims 2 and 3 under 35 U.S.C. §103(a) as anticipated by Akiyama in view of Tanaka is in error regarding the characterization of Akiyama as providing motivation for one of skill in the art to combine Akiyama with Tanaka to obtain a transistor in which a distance between a first main surface and an interface is 200 μm or less.[1]

First, Appellant notes that substrate thickness is not mentioned at all by Tanaka. Thus, Tanaka does not mention any thickness between a first main surface and an interface, as those features are recited in Claims 2 and 3. Thus, the rejection relies on Akiyama as teaching those features.

Further, Akiyama merely describes a device that has a structure including an alternating N/P type impurity region doped within a substrate to a depth of 30 μm. Akiyama

[1] Office Action mailed April 18, 2006, at page 4, lines 8-16.

also indicates that a thickness of the remaining portion of the substrate, including a N^- type region, and N^+ and P^+ IGBT regions is 190 μm. Although Akiyama does not describe the fabrication process used to make such a device, Appellant respectfully submits that it would have been clear to one of skill in the art of semiconductor device fabrication that regardless of whether the device of Akiyama was made by impurity diffusion or ion implantation, the initial wafer thickness would be 220 μm. That is because, as known in the art, semiconductor fabrication process steps that change an impurity concentration in a semiconductor substrate, such as diffusion or implantation process steps, do not substantially increase a thickness of the wafer. Instead, such process steps change a concentration of an impurity ***within*** a region that is inside and between the main surfaces of an existing semiconductor wafer. In other words, impurity regions, such as the N/P regions shown in Akiyama's Fig. 1a, are not attached to a substrate. Instead, such impurity regions are formed ***within*** an existing substrate by adding impurities to existing portions of a substrate.

Accordingly, it would have been clear to one of skill in the art that a process of making the semiconductor device described by Akiyama would begin with a wafer having a thickness of 220 μm, into which N and P type impurities might be added (e.g., by diffusion or implantation) such that the impurities would reach into the existing substrate at a depth of 30 μm. Further, although Akiyama indicates that the 220 μm wafer shown in Fig. 1a includes a 190 μm thick remaining portion including the N^- type region and the IGBT regions, as well as a 30 μm thick N/P region, Akiyama is silent regarding any advantages for selecting the thicknesses of those regions, and Akiyama does not teach or suggest any device properties related to those region thicknesses. In addition, Akiyama only describes a wafer having a thickness of 220 μm and does not describe or otherwise suggest any other wafer having a different thickness or suggest any step or motivation for reducing a thickness of the wafer.

As noted above, Tanaka is completely silent regarding a thickness of a wafer, and in FIGs. 10 and 11, Tanaka illustrates a device having N/P regions 12 and 2B that are implanted ***into*** an existing semiconductor substrate 1 up to a depth of 0.8 μm.[2] Further, Tanaka does not describe the thickness of semiconductor substrate 1 or indicate any reason to reduce the thickness of the substrate.

Appellant respectfully traverses the assertion in the Office Action that

> it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Akiyama by using a thickness of less than 1 micron for the first and second semiconductor regions as taught by Tanaka . . . Furthermore, when the thickness of the first and second semiconductor regions as taught by Tanaka is incorporated into the device of Akiyama, the distance between said first main surface and said interface is 200 microns or smaller (190 microns + 0.8 microns).[3]

First, Appellant notes that if one were to combine the teachings of Tanaka and Akiyama, without adding additional steps that are not taught or suggested in the references, one would not obtain the claimed invention. As described above, Akiyama only describes a wafer thickness of 220 μm and an N/P impurity depth of 30 μm. Further, Appellant respectfully points out that changing a first wafer thickness to a different, smaller wafer thickness, would ***require additional process steps***, not fewer process steps. For example, extra polishing or etching steps would be required to remove wafer material and reduce a thickness of a wafer from 220 μm to 200 μm. The references in the Office Action are silent regarding any such process steps or any motivation to perform such extra steps. Therefore, although there is no motivation to do so, if one of skill in the art were to combine the teachings of Tanaka with Akiyama, the combined teaching would indicate to N/P regions to a depth of 0.8 μm within an existing 220 μm substrate, which is larger than the 200 μm maximum distance recited in Claims 2 and 3. Akiyama does not teach or suggest any other wafer thickness.

---

[2] Tanaka at page 10, paragraph [0187].
[3] Office Action mailed April 18, 2006, at page 4, lines 8-10 and 13-16.

As noted in the specification and as described above, the Appellant discovered specific advantages that may be achieved by maintaining the claimed distance of 200 μm or smaller. However, Tanaka and Akiyama are silent regarding those advantages, and do not describe any wafer having a thickness of 200 μm or smaller. For one to obtain a wafer thickness of 200 μm or smaller starting with the 220 μm thick wafer described by Akiyama, one would have to perform additional steps, such as etching or polishing, to remove wafer material, and such steps, or even motivation to perform such steps, are absent from the applied references.

Further, Appellant respectfully notes that one of skill in the art would not assemble a semiconductor device by starting with a 190 μm semiconductor substrate and adding a 0.8 μm N/P impurity region to obtain a wafer having a thickness of 190.8 μm, as suggested in the Office Action.[4] As discussed above, one of skill in the art would have known that impurity regions are added to existing semiconductor substrates by diffusion or implantation, without substantially increasing the wafer thickness. Thus, to obtain a wafer with a 190 μm region (i.e., including the N^- region and the IGBT region) and a 0.8 μm N/P impurity region, as proposed by the Office Action, one of skill in the art would start with a wafer having a thickness of 190.8 μm, and Appellant respectfully submis that the references in the Office Action do not teach or suggest any wafer having that thickness. Further, there is no motivation or reason mentioned in the applied references for performing any additional steps to reduce a thickness of a wafer or to use a different wafer thickness other than the 220 μm thick wafer described in Akiyama. Accordingly, it appears that the suggestions in the Office Action represent improper hindsight reasoning based only on Appellant's disclosure.

Further, Appellant respectfully traverses the assertion in the Office Action that "Applicant has suggested an additional modification to Akiyama, where the thickness of the

[4] Office Action mailed April 18, 2006, at page 4, line 13-16.

N- region is increased from 190 μm to 220 μm."[5] However, as noted above, Akiyama does not teach or suggest an N- region having a particular thickness. Instead, Akiyama shows a depth of impurities in the N/P region, and shows a total dimension of the remaining portions of the wafer, including the N^- region and the N^+ and P^+ IGBT regions. Accordingly, contrary to that assertion in the Office Action, Appellant has suggested no modification to a thickness of an N- region in Akiyama at least because there is no teaching of an N^- region thickness in Akiyama or Tanaka.

Further, Akiyama does not teach or suggest fabricating a device by starting with a 190 μm N- substrate/IGBT region and adding to that an additional 30 μm N/P region, because as one of skill in the art knows, impurity regions are not commonly added or attached to each other. Further, contrary to the assertions in the Advisory Action,[6] if such regions are attached to one another, or grown by some additional process, that attachment or growth process would require additional process steps not disclosed or suggested by the references. Instead, one of skill in the art would have known that impurities are normally added within an existing portion of a substrate to create an impurity region within the existing substrate without changing the substrate thickness. Thus, contrary to the assertion in the Office Action,[7] Appellant does not suggest that one of skill in the art would take steps to ***increase*** an N- region if Akiyama and Tanaka were combined. On the other hand, Appellant points out that no change in the dimensions of thickness of a remaining portion of a wafer (as measured by Akiyama) would be the normal and expected outcome if one of skill in the art were to combine the teachings of Akiyama and Tanaka. That is, if the artisan was to insert an impurity region having a depth of 1 μm or less (i.e., the depth taught by Tanaka) within a 220 μm semiconductor substrate (i.e., the wafer thickness taught by Akiyama), the resulting substrate thickness would still be approximately 220 μm.

[5] Office Action mailed April 18, 2006, at page 8, lines 18-19.
[6] Advisory Action mailed July 31, 2006, at continuation sheet, lines 4-5.
[7] Office Action mailed April 18, 2006, at page 8, lines 18-19.

In addition, Appellant traverses the assertion in the Advisory Action that because Akiyama "deliberately shows a straight line separating the N+/P+ regions from the N- region. . . . the N- region is a separate and distinct layer [and] the regions are not all formed from the same wafer." However, the Advisory Action provides no support for this conclusion, and Appellant respectfully submits that one of skill in the art would not reach the same conclusion at all. First, there is absolutely no support or suggestion in the references for the Examiner's idea of forming an active portion of a device from plural wafers. Second, such an approach would certainly require additional steps that are also not disclosed or suggested, even if such an approach were feasible.

In addition, Appellant traverses the assertion in the Advisory Action that the wafer thickness is a result effective variable because "a smaller substrate means a smaller device."[8] However, there is no teaching or suggestion in the applied references that a reduction of a width of a semiconductor substrate would advantageously result in a "smaller device." Further, although a footprint area of a semiconductor device does affect a resulting device size, Appellant respectfully submits that one of skill in the art would not have understood the ***thickness*** of a semiconductor substrate to be a variable that affects the size of a device. Accordingly, neither the Advisory Action, nor the applied references supply any reason for concluding that the thickness of a substrate is a result effective variable.

Further, Appellant points out that Akiyama does not teach or suggest a N^- region plus IGBT portion that exists independent of the wafer or independent of other layers in the wafer, or a N^- region that other layers can be added on top of or beneath. Instead, Akiyama merely shows an example of a 220 μm thick wafer having a 30 μm thick N/P impurity layer, which leaves 190 μm for remaining layers (e.g., N^- impurity layer, IGBT P^+ base layer and N^+ layer). If an artisan were to change the depth of the N/P impurity layer described by

[8] Advisory Action at continuation page, line 11.

Akiyama from 30 μm to 1 μm, as the Office Action asserts is suggested by Tanaka, the artisan would obtain a 220 μm thick wafer having a 1 μm thick N/P impurity layer and 219 μm left for remaining layers.

Thus, it is clear that Akiyama and Tanaka, if combined as suggested in the Office Action, merely describe a semiconductor device having a wafer thickness of 220 μm, which is greater than the maximum claimed distance. Accordingly, Appellants respectfully submit that Akiyama and Tanaka do not teach or suggest "a distance between said first main surface and said interface is equal to 200 μm or smaller," as recited in independent Claims 2 and 3.

Therefore, Appellant respectfully submits that independent Claims 2 and 3, and claims depending therefrom, patentably define over Akiyama and Tanaka, whether taken individually or in combination.

Accordingly, Appellant respectfully submits that the rejection of Claims under 35 U.S.C. § 103(a) as unpatentable over Akiyama and Tanaka should be reversed.

Further, Appellant respectfully submits that the rejection of Claims 5 and 14 under 35 U.S.C. § 103(a) as unpatentable over Akiyama in view of Tanaka and Reznik is also in error. Claims 5 and 14 depend from Claims 2 and 3, which as discussed above are believed to patentably define over Akiyama and Tanaka. Further, Reznik does not teach or suggest and is not relied upon for the claimed features lacking in the disclosures of Akiyama and Tanaka.

Accordingly, Appellant respectfully requests that the rejection of Claims 5 and 14 under 35 U.S.C. § 103(a) as unpatentable over Akiyama in view of Tanaka and Reznik also be reversed.

B) Tanaka fails to teach or suggest a distance between a first main surface and an interface is 200 μm or less, as recited in Claims 2 and 3, and fails to provide motivation regarding such a thickness.

Appellant respectfully submits that the rejection of Claims 1-3, 6 and 15 under 35 U.S.C. § 103(a) as unpatentable over Tanaka is in error regarding the assertion that it would

have been obvious to one of skill in the art to have a distance between the first surface and the interface equal to or less than 200 μm.[9]

First, as discussed above, independent Claims 2 and 3, and claims depending therefrom, are believed to patentably define over Tanaka. Moreover, Claim 1 was previously canceled.

In addition, Appellant respectfully traverses the assertion in the Office Action that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a distance between the first surface and the interface equal to or less than 200 microns, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art."[10] The present inventors discovered the importance of controlling the wafer thickness, and as discussed above, Tanaka is silent regarding a thickness of a wafer.

In particular, as discovered by the present inventors, the wafer should advantageously be 200 μm or smaller in an IGBT with a built-in freewheeling diode to avoid undesirable increases in Vf and VCE(sat) as shown in Figures 4-8 of the present application, and as described in the specification at page 18, line 5, to page 19, line 6. For example, Figure 4A shows that VCE(sat) increases dramatically for values of wafer thickness greater than 200 μm.

On the other hand, Tanaka does not teach or suggest that a thickness of a wafer is even a relevant consideration. Thus, it is clear that Tanaka does not indicate or suggest that the thickness of a wafer is a "result effective variable." Appellant respectfully submits that finding motivation in Tanaka to vary a thickness of a wafer is impermissible hindsight reasoning, as discussed above.

---

[9] Office Action mailed April 18, 2006, at page 7, lines 7-10.
[10] Office Action at page 7, lines 7-11.

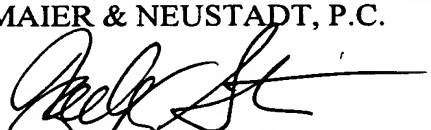
Accordingly, Appellant respectfully requests the rejection under 35 U.S.C. § 103(a) of Claims 1-3, 6 and 15 as unpatentable over Tanaka also be reversed.

CONCLUSION

The rejections applied to Claims 2-6 and 13-15 should be reversed as being clearly improper under the controlling precedent cited above and for the above-noted reasons.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Zachary S. Stern
Registration No. 54,719

GJM:ZSS
I:\ATTY\ZS\25's\252\252069US\252069 APPEAL BRIEF.091406.DOC

VII. CLAIMS APPENDIX 37 C.F.R. § 41.37(c)(1)(viii)

Claim 2 (Previously Presented): An insulated gate bipolar transistor comprising:

a semiconductor substrate of a first conductivity type including a first main surface and a second main surface;

an insulated gate transistor formed in a region of said semiconductor substrate on a side of said semiconductor substrate where said first main surface is included, said insulated gate transistor including a channel of said first conductivity type which is formed within a base region of a second conductivity type during an on state of said insulated gate transistor, said base region extending from said first main surface toward an interior of said semiconductor substrate;

a first main electrode formed on said first main surface and being in contact with said base region of said insulated gate transistor at said first main surface;

a first semiconductor layer of said first conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor;

a second semiconductor layer of said second conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor; and

a second main electrode formed on said first semiconductor layer and said second semiconductor layer,

wherein an interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer is parallel to said first main surface,

a distance between said first main surface and said interface is equal to 200 μm or smaller,

a thickness of each of said first semiconductor layer and said second semiconductor layer is equal to 2 μm or smaller, and

a first interface between said first semiconductor layer and said second main electrode occupies 20-70% of said interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer.

Claim 3 (Previously Presented): An insulated gate bipolar transistor comprising:

a semiconductor substrate of a first conductivity type including a first main surface and a second main surface;

an insulated gate transistor formed in a region of said semiconductor substrate on a side of said semiconductor substrate where said first main surface is included, said insulated gate transistor including a channel of said first conductivity type which is formed within a base region of a second conductivity type during an on state of said insulated gate transistor, said base region extending from said first main surface toward an interior of said semiconductor substrate;

a first main electrode formed on said first main surface and being in contact with said base region of said insulated gate transistor at said first main surface;

a first semiconductor layer of said first conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor;

a second semiconductor layer of said second conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor; and

a second main electrode formed on said first semiconductor layer and said second semiconductor layer,

wherein an interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer is parallel to said first main surface,

a distance between said first main surface and said interface is equal to 200 μm or smaller,

a thickness of each of said first semiconductor layer and said second semiconductor layer is equal to 2 μm or smaller, and

a second interface between said second semiconductor layer and said second main electrode occupies 30-80% of said interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer.

Claim 4 (Previously Presented): The insulated gate bipolar transistor according to claim 2,

wherein a total width of a first width of said first semiconductor layer and a second width of said second semiconductor layer which are parallel to said first main surface and extend along a direction in which said first semiconductor layer and said second semiconductor layer are aligned is in a range from 50 μm to 200 μm.

Claim 5 (Previously Presented): The insulated gate bipolar transistor according to claim 2,

wherein said semiconductor substrate includes an additional semiconductor layer of said first conductivity type which extends from an interface between said base region and said semiconductor substrate toward said interior of said semiconductor substrate, and an impurity concentration of said additional semiconductor layer is higher than that of a portion of said semiconductor substrate which forms an interface with said additional semiconductor layer.

Claim 6 (Previously Presented): An inverter circuit comprising:

the insulated gate bipolar transistor according to claim 2,

wherein said insulated gate bipolar transistor functions as a switching device with a built-in freewheeling diode.

Claim 7 (Withdrawn): A method of manufacturing an insulated gate bipolar transistor, comprising the steps of:

forming an MOSFET cell in a region of a semiconductor substrate of a first conductivity type on a side of said semiconductor substrate where a first main surface thereof is included;

forming a first semiconductor layer of said first conductivity type and a second semiconductor layer of a second conductivity type adjacent to said first semiconductor layer such that each of said first and second semiconductor layers extends from a portion of a second main surface of said semiconductor substrate which faces said MOSFET cell toward an interior of said semiconductor substrate, after forming said MOSFET cell; and

forming a second main electrode in contact with said first and second semiconductor layers on said second main surface comprising said first and second semiconductor layers formed thereon.

Claim 8 (Withdrawn): The method of manufacturing an insulated gate bipolar transistor according to claim 7,

wherein a first main electrode and said second main electrode are formed on said first main surface and on said second main surface of said semiconductor substrate, respectively, after forming said first and second semiconductor layers.

Claim 9 (Withdrawn): The method of manufacturing an insulated gate bipolar transistor according to claim 7, further comprising the step of:

polishing said semiconductor substrate from said second main surface to make a thickness of said semiconductor substrate equal to 200 μm or smaller after forming said MOSFET cell and before forming said first and second semiconductor layers.

Claim 10 (Withdrawn): The method of manufacturing an insulated gate bipolar transistor according to claim 9, further comprising:

forming a projection serving as a mask alignment mark in a region of said semiconductor substrate on a side of said semiconductor substrate where said second main surface is included, after polishing said semiconductor substrate and before forming said first and second semiconductor layers.

Claim 11 (Withdrawn): The insulated gate bipolar transistor according to claim 5, wherein said insulated gate transistor includes a trench MOSFET cell.

Claim 12 (Previously Presented): The insulated gate bipolar transistor according to claim 2, further comprising:

an interposed portion of the semiconductor substrate being in contact with said second main electrode and interposed between the first semiconductor layer and the second semiconductor layer.

Claim 13 (Previously Presented): The insulated gate bipolar transistor according to claim 3,

wherein a total width of a first width of said first semiconductor layer and a second width of said second semiconductor layer which are parallel to said first main surface and extend along a direction in which said first semiconductor layer and said second semiconductor layer are aligned is in a range from 50 μm to 200 μm.

Claim 14 (Previously Presented): The insulated gate bipolar transistor according to claim 3,

wherein said semiconductor substrate includes an additional semiconductor layer of said first conductivity type which extends from an interface between said base region and said semiconductor substrate toward said interior of said semiconductor substrate, and an impurity concentration of said additional semiconductor layer is higher than that of a portion of said semiconductor substrate which forms an interface with said additional semiconductor layer.

Claim 15 (Previously Presented): An inverter circuit comprising:

the insulated gate bipolar transistor according to claim 3,

wherein said insulated gate bipolar transistor functions as a switching device with a built-in freewheeling diode.

Claim 16 (Previously Presented): The insulated gate bipolar transistor according to claim 3, further comprising:

an interposed portion of the semiconductor substrate being in contact with said second main electrode and interposed between the first semiconductor layer and the second semiconductor layer.

Claim 17 (Previously Presented): The insulated gate bipolar transistor according to claim 14, wherein said insulated gate transistor includes a trench MOSFET cell.

IX. EVIDENCE APPENDIX UNDER 37 C.F.R. § 41.37(c)(1)(ix)

None.

X. RELATED PROCEEDINGS APPENDIX UNDER 37 C.F.R. § 41.37(c)(1)(x)

None.